**WHAT IS CLAIMED IS:**

1. A method of generating a voltage internally by a memory device, comprising:

generating, internally to the memory device, a negative voltage with respect to a ground reference;

applying the negative voltage to a portion of an array of memory cells;

obtaining temperature information indicative of the temperature of the memory device; and

varying the level of the negative voltage based on the temperature information.

2. The method of claim 1, wherein applying the negative voltage to a portion of an array of memory cells increases a threshold voltage level of one or more memory cells.

3. The method of claim 2, wherein applying the negative voltage to a portion of an array of memory cells comprises applying the negative voltage to a substrate of switching transistor one or more memory cells.

4. The method of claim 2, wherein applying the negative voltage to a portion of an array of memory cells comprises applying the negative voltage to a wordline of one or more memory cells when the one or more memory cells are deactivated.

5. The method of claim 1, wherein obtaining temperature information comprises reading one or more bits in a mode register.

6. The method of claim 5, wherein a refresh rate of the memory device is also varied based on the one or more bits.

7. The method of claim 1, wherein obtaining temperature information comprises measuring the temperature of the memory device with an internal temperature sensor.

8. The method of claim 1, wherein varying the level of one or more internally generated voltages based on the temperature information comprises:

generating one or more control signals based on the temperature information; and

adjusting, based on the one or more control signals, at least one of an output voltage level of a detector or an output voltage level of a reference, wherein both the detector and the reference are part of a voltage generator.

9. A method of biasing a switching transistor of one or more memory cells of a memory device, comprising:

generating, from a supply voltage, a bias voltage to be applied to a substrate of a switching transistor of one or more of the memory cells; and

varying the level of the bias voltage based on temperature information indicative of a temperature of the memory device.

10. The method of claim 9, wherein the bias voltage is negative with respect to a ground reference and increases a threshold voltage of the one or more memory cells.

11. The method of claim 10, wherein varying the level of the bias voltage based on temperature information comprises decreasing the level of the bias voltage as device temperature increases.

12. The method of claim 11, wherein varying the level of the bias voltage based on temperature information comprises adjusting the output level of at least one of a voltage detector and a voltage reference based on the temperature information.

13. The method of claim 12, wherein increasing the output level of at least one of a voltage detector and a voltage reference comprises shunting a resistor of a voltage divider circuit.

14. The method of claim 9, further comprising generating a negative wordline voltage, to be applied to a wordline of one or more memory cells when the wordline is deactivated, using the bias voltage as a supply voltage.

15. The method of claim 14, further comprising varying the level of the negative wordline voltage based on the temperature information.

16. The method of claim 9, wherein:

the temperature information is supplied as bits in a mode register; and

a refresh rate of the memory device is also varied based on the temperature information.

17. The method of claim 9, wherein the temperature information is generated by a temperature sensing component internal to the memory device.

18. A memory device comprising:

a plurality of memory cells;

means for supplying temperature information indicative of a temperature of the memory device; and

a voltage generator to generate a bias voltage negative with respect to a ground reference to be applied to a substrate of a switching transistor of one or more of the memory cells, wherein the voltage generator is configured to vary the level of the bias voltage based on the temperature information.

19. The memory device of claim 18, wherein the voltage generator is configured to lower a level of the bias voltage as the temperature of the memory device increases.

20. The memory device of claim 18, wherein the voltage generator varies the level of the bias voltage in response to a plurality of temperature control signals generated based on the temperature information.

21. The memory device of claim 20, wherein:

distinct logic states of the control signals corresponds to distinct temperature ranges; and

the voltage generator is configured to adjust the bias voltage to a different level for each distinct temperature range.

22. The memory device of claim 18, wherein:

the voltage generator comprises a voltage detector and a voltage reference; and

the voltage generator is configured to vary the level of the bias voltage by varying an output voltage of at least one of the voltage detector and the voltage reference.

23. The memory device of claim 18, further comprising a voltage regulator to generate a negative wordline voltage based on the bias voltage.

24. The memory device of claim 18, wherein the voltage regulator is configured to vary a level of the negative wordline voltage based on the temperature information.

25. A memory device comprising:

a plurality of memory cells;

means for supplying temperature information indicative of a temperature of the memory device; and

a voltage regulator to generate a negative wordline voltage to be applied to a wordline of one or more of the memory cells, wherein the voltage generator is

configured to vary the level of the negative wordline voltage based on the temperature information.

26. The memory device of claim 25, further comprising one or more mode registers containing the temperature information.

27. The memory device of claim 25, further comprising an internal thermometer configured to supply the temperature information.

28. The memory device of claim 25, wherein the memory device further comprises a voltage generator configured to generate a negative bias voltage to be supplied to a substrate of one or more of the memory cells; and

the voltage regulator is configured to generate the negative wordline voltage using the negative bias voltage as a supply voltage.